GIGABIT LOGIC PROSPECTS OF GaAs E-JFET INTEGRATED CIRCUITS*

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ABSTRACT

Computer simulation and experimental results will be presented for a 1 μm GaAs enhancement mode JFET. Logic performance of 250 ps propagation delay time with a power dissipation of 200 μW/gate at a fan-out of 3 offers gigabit logic for LSI, i.e. delay-power product of 50 fJ. A planar integration will be described which utilizes selective ion implantation of n- and p- impurities for the channel and pn-junction gate formation in semi-insulating GaAs substrate material.

Introduction

The GaAs enhancement mode (normally-off) field-effect transistor has an excellent potential for use as the basic logic element in low-power high speed integrated circuits.[1, 2] While the enhancement mode MESFET[1] has only a logic swing of 0.4 volts and has a poor noise immunity, the enhancement mode J-FET operates with a logic swing of 0.8 to 1.0 volt and good noise immunity. Gigabit logic prospects of 1 μm channel GaAs E-JFET's will be demonstrated by computer simulation of optimized logic gate configurations. Experimental results, which were obtained from small-scale integrated circuits will be presented and correlated with those predicted from computer solutions. A planar integration technology will be described which utilizes ion implantation of n- and p-type impurities for the n-channel and pn-junction gate formation in semi-insulating GaAs substrate material. Based on these results, projections for MSI and LSI capability and logic performance of this planar technology will be assessed.

Device Characteristics

For circuit analysis a model is required for the E-JFET. Experimental values of voltage-current and capacitance relations were established for known geometries and utilized in computer simulations. The voltage-current capability of the GaAs E-JFET can be assessed from the relation[3]

$$I_{DS} = K(V_G - V_T)^2 \qquad (1)$$

where $K = K'_o(W/L) = \varepsilon\varepsilon_o\mu W/2aL$. With $\mu = 4000\ cm^2/Vs$ and $a = 1000A$ the theoretical value for $K' = 2 \times 10^{-4} A/V^2$. Experimental values for 1 μm channel devices have established values of $K' = 1 \times 10^{-4} A/V^2$. This value is very encouraging and reasonable in view of the uncertainty of the channel height a not being well defined in the devices with ion implanted impurity profiles. For all computer simulations this experimental value of K' has been used to predict the circuit performance. Because of the low voltage operation no appreciable hot electron effects[4] are expected in the E-JFET with L = 1 μm and advantage of the low field high mobility of n-type GaAs is retained for improved circuit performance. A typical voltage-current characteristic of a device with W = 100 μm and L = 1 μm is presented in Figure 1. For scaling purposes one can deduce a current drive capability of 80 μA/μm (2 mA/mil) at V_G = 1 volt.

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Logic Gate Design

A circuit analysis was performed using the ASTAP and NET-2 programs[5] to investigate switching performance of E-JFET logic gates. The goal was to find the optimum circuit configuration for a maximum dc power dissipation of 200 μW per unit gate, based on a 50/50% off-on condition.

The optimum system speed is obtained when rise time (t_r) and fall time (t_f) at the output of the gate are equal. The circuit optimization, consequently, was aimed at obtaining minimum and equal rise and fall times, and minimum propagation delay (t_{pd}). Another consideration in the optimization was the desire to be compatible with the 1 GHz clock rate expected for future high-speed data processing systems. For this rate, the sum of ($t_r + t_{pd}$) or ($t_f + t_{pd}$) should not exceed the width of the clock period, or 1 nanosecond. In systems using ECL and T^2L logic circuits, propagation delay is generally several times larger than rise or fall time. In low-voltage, high-speed GaAs logic circuits, t_{pd} is usually a fraction of t_r or t_f. Therefore, in assessing the overall system speed, t_r and t_f as well as t_{pd} must be taken into account.

Optimized Logic Gate

Since p-channel technology of E-JFETs is excluded for high speed circuit design because of the low mobility of holes in GaAs, the analyses were confined to n-channel E-JFET circuits only. Three circuits were examined: a) the E-JFET inverter with resistive load (Figure 2a), b) the E-JFET inverter with depletion JFET load (Figure 2b) and c) the E-JFET inverter in quasi-complementary design with resistive pull-up (Figure 2c). In order to compare the relative performance of each configuration on a common basis, the dc power dissipation was kept constant at approximately 200 μW. Values of gate-drain and gate-source junction capacitances become extremely small with gate geometries of less than 1 x 50 μm. For example, capacitances for 1 x 10 μm geometry are: C_{gs} = 9.5 fF, C_{gd} = 3.6 fF, and C_{ds} = 6.3 fF. The latter is primarily a function of source-drain contact areas, leading to a trade-off between drain-source capacitance and contact resistance. For geometries under 10 μm width, the fringing capacitance at the edges of the channel becomes increasingly important. For a contact length of 5 μm, gate width of 1 μm, the drain-source fringing capacitance was measured to be 1 fF. This value was determined by measuring several larger metalization patterns of different width and sealing the results.

For the circuit analyses, the inverting transistor of the resistive load inverter, the depletion load inverter and Q_1 of the quasi-complementary inverter had a gate size of 1 x 12 μm. Table 1 gives the results

of the analyses. Comparison of t_{pd} values for the three circuits shows that the depletion-load and resistive load inverters are slightly faster than the quasi-complementary (Q-C) circuit for a fan-out of 1 and 2. For fan-outs higher than 2, the resistive load circuit is of limited usefulness since the long rise time and added propagation delay approaches one nanosecond. The depletion load inverter shows the best speed, but its rise time starts to deteriorate at fan-outs greater than five. The quasi-complementary circuit performs at almost the same speed as the latter, however is capable of driving almost twice the load capacitance, C_{LOAD}. For C_{LOAD}>150 fF, a quasi-complementary inverter-buffer of larger geometry and power dissipation should be used when using a 1 GHz clock. The optimum IC design should probably be implemented with a mixture of resistive load or depletion load inverters and quasi-complementary inverters. Addition of the depletion loads to the IC requires an additional processing step, which would consist of a separate n-implant of greater depth than for the enhancement devices. The results of the analyses show that the Q-C circuit provides the best overall performance of the three inverters. Gates constructed with this configuration can be operated at clock speeds of 1 GHz or above, depending upon fan-out.

TABLE 1

Comparison of Switching Times for Three Inverter Circuits

Configuration	t_r(ps)	t_f(ps)	t_{pd}(ps)	Fan-Out	C_{LOAD}(fF)
E-JFET Resistive Load V_{DD} = 1.25V P_d = 165 µW	340	160	88	1	16
	700	310	188	3	48
	950	390	285	5	81
	1775	900	538	10	162
E-JFET Depletion Load V_{DD} = 1.5V P_d = 240 µW	220	120	85	1	16
	430	240	173	3	48
	610	360	260	5	81
	1100	700	475	10	162
E-JFET Quasi-Complementary, resistive pull-up V_{DD} = 1.5V P_d = 202 µW	450	200	160	1	30
	510	380	253	3	90
	610	560	338	5	150
	975	1025	550	10	300

Note: $P_d = (P_{d(ON)} + P_{d(OFF)})/2$

Quasi-complementary circuit inverters with 1 µm and 2.5 µm gate length were tested. The gate widths for $Q_{1,23}$ was 25, 50 and 50 µm for the 1 µm geometries; and 75, 150 and 150 µm for the 2.5 µm geometries. Calculated and measured voltage transfer characteristics of an optimized quasi-complementary are plotted in Figure 3. The actual device shows a slightly lower threshold voltage which accounts for the earlier drop in output voltage at approximately 0.2V.

In Table 2, the calculated values for logic swing (V_{1-0}), input voltage to produce a 10 to 90% change in output voltage ($V_{IN(10-90)}$), dc gain in the transition region of 10 to 90% of output voltage ($A_{V(10-90)}$) noise margin with high input (V_{MH}) and noise margin with low output (V_{ML}) are compared with measured values for the 5-input NOR gate and/or quasi-complementary inverter.

TABLE 2

Measured and Calculated Voltage Transfer Parameters

(All Values in Volts, V_{DD} = 1.5V)

DEVICE \ PARAMETER	V_{1-0}	$V_{IN(10-90)}$	$A_{V(10-90)}$	V_{MH}	V_{ML}
Calculated (Unoptimized Geometries)	1.12	.152	7.33	.314	.649
Typical Device Wafer 205-2	1.17	.370	3.16	.110	.690
Typical Device Wafer 205-3	1.04	.410	2.03	.340	.290
Calculated (Optimized Geometries)	1.15	.267	3.45	.360	.523
SDFL (Ref. 7) Depletion MESFET Logic (Low Power)	.750	.270	2.22	.370	.110
E-MESFET (Ref. 8) Logic (Low Power)	.600	.270	2.22	.060	.270
D-MESFET (Ref. 6) Logic (High Power)	2.700	.296	2.7	.750	.900

The comparison with other GaAs FET logic gate families shows that E-JFET logic has higher logic swings and larger noise margins than comparable low-power logic gates using depletion MESFET's. However, high-power MESFET logic shows better noise margins at the expense of much higher power dissipation. E-JFET gates within the design margin of threshold voltage give also higher gain in the active region. These results demonstrate that the use of enhancement devices is technically sound and will lead to excellent logic performance.

Planar Processing Technology

A planar fabrication technology for E-JFET integrated circuit was developed which utilizes selected ion implantation of n- and p-type impurities into semi-insulating GaAs substrate material. Combined with a two-level metalization small-scale integrated circuits, such as the positive edge triggered flip-flop shown in Figure 4, were fabricated and electrically evaluated. For 2.5 µm channel length devices the gate junction formation was accomplished with Zn diffusion. At 1 µm channel length, as used for all designs now, the detrimental lateral spread of diffusion is eliminated by using Mg^+ ion implantation. Figure 5 is a SEM picture of the Si_3N_4 channel opening of 1.1 µm through which the Mg^+ implantation takes place. The openings are plasma-etched using photolithography. With E-beam technology the process is readily extended to 0.5 µm device structures. A SEM photograph of a section of the positive edge-triggered flip-flop, whose logic diagram is shown in Figure 4, is presented in Figure 6. Planar device structure, passivated with Si_3N_4, of 2.5 and 1.0 µm channel length and associated two-level metalization, are discernible.

Summary and Conclusion

An all ion implanted planar E-JFET technology was established for 1 µm channel integrated circuit fabrication. Current driving capabilities of GaAs E-JFET's offer the design of optimized logic gates with a delay-

power product of 31 and 51 fJ for the resistive load and quasi-complementary inverter, respectively. Computer simulations determined the optimized logic gate configuration and gigabit logic performance is predicted. Various integrated circuits with 1 μm channel devices, optimized for minimum power dissipation at the optimum propagation delay time, were designed and fabricated. They are in electrical evaluation to correlate experimental performance characteristics with those predicted from computer simulations. Projections of MSI and LSI capabilities of GaAs E-JFET's will be based on these results.

With further improvements in the planar processing technology an integrated logic is achievable in the 1-2 Gbit/s range, operating at a power dissipation of 200 μW/gate. This qualifies for the prerequisite of LSI with 3000 gates on a chip and a safe total power dissipation of 600 mW. A quasi-complementary gate occupies an area of about 1 mil^2. Assuming that the final circuit layout on the chip consumes 80% of the area with interconnections, a chip size of 120 x 120 mil^2 would suffice to accommodate the 3000 logic gate functions.

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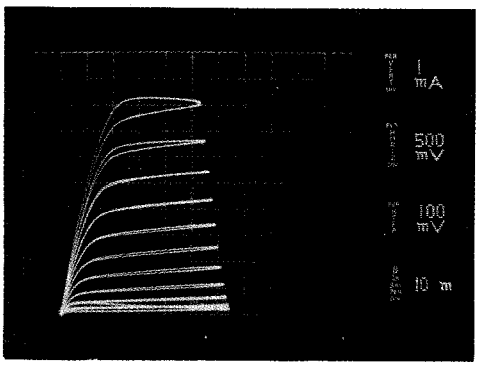


FIGURE 1: VOLTAGE-CURRENT CHARACTERISTIC OF 1 μm CHANNEL GaAs E-JFET WITH W = 100 μm FROM LOT C-187.
(MAX. V_G = + 1V)

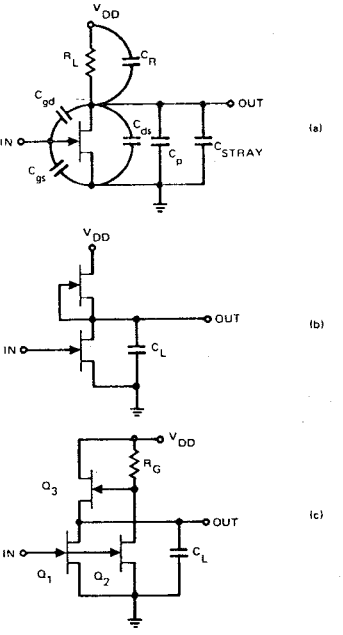


FIGURE 2: INVERTER CIRCUITS WITH VARIOUS LOAD CONFIGURATIONS

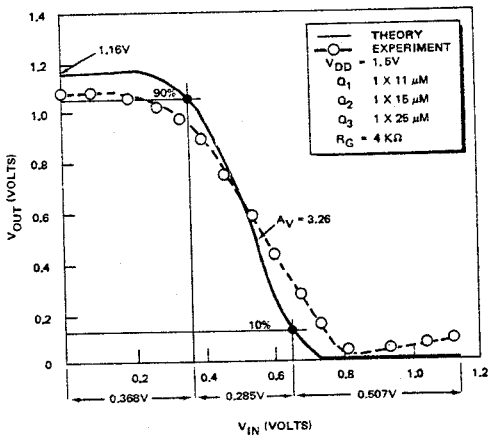
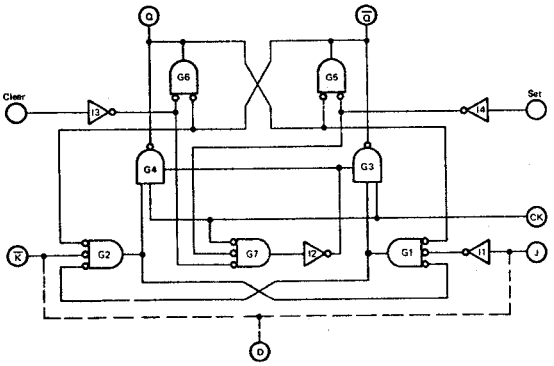
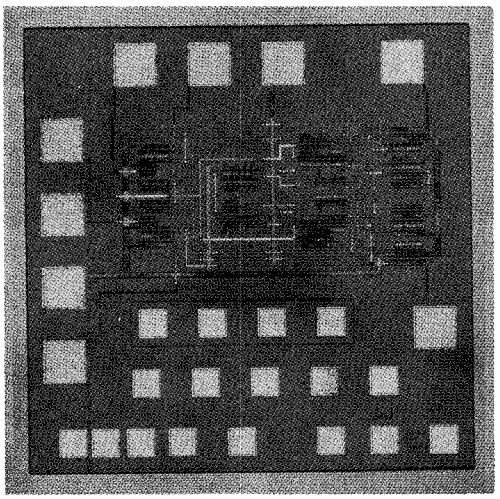


FIGURE 3: CALCULATED AND MEASURED VOLTAGE TRANSFER CHARACTERISTICS.



a) LOGIC DIAGRAM



b) MICROPHOTOGRAPH OF CHIP (30 x 30 mil^2)

FIGURE 4: POSITIVE EDGE-TRIGGERED FLIP-FLOP DASHED CONNECTION YIELDS A TYPE D FLIP-FLOP.

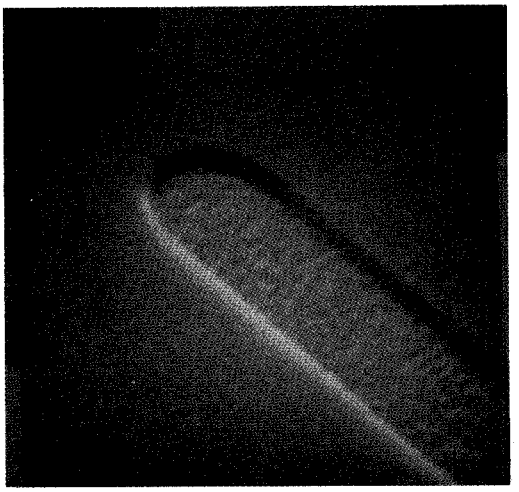


FIGURE 5: SEM PHOTOGRAPH OF 1.1 μm PLASMA ETCHED CHANNEL OPENING IN Si_3N_4. MAG. x 20,000.

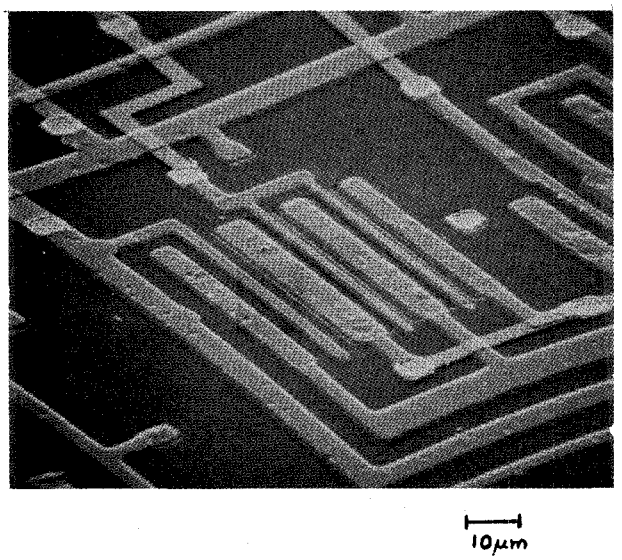


FIGURE 6: SEM PHOTOGRAPH OF PLANAR IC TECHNOLOGY WITH 2.5 AND 1.0 μm CHANNEL DEVICES, MAG. x 1,000